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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/903,059	07/10/2001	Constantin Bulucea	NS-4971 US	9375

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EXAMINER
FARAHANI, DANA

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,059	BULUCEA, CONSTANTIN	
	Examiner	Art Unit	
	Dana Farahani	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 3, 8, 10, 11, 22, 31-34, 36, 37, and 42, are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda et al., hereinafter Ikeda (U.S. 5,497,028).

Regarding claims 1 and 2, Ikeda discloses in figure 50C, a structure comprising: a varactor comprising (a) a plate region at the top right of the figure and a body region at the right center of the figure of a semiconductor body, (b) a plate electrode and a body electrode corresponding to the plate region and the body region, respectively, connected to the plate and body regions, (c) a dielectric layer, not shown, but inherent to the gate of the transistor, situated over the semiconductor body and contacting the body region, and (d) a gate electrode shown as the bubble connecting the gate to the top inductor situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, not shown but inherent to the structure of the transistor, the plate and body regions meeting each other to form a p-n junction, shown at the right center of the figure as an arrow connected to the plate region, a surface depletion region of the body region extending along the dielectric layer below the gate electrode and being spaced apart from a body contact portion of the body region, the body contact portion contacting the body electrode and being more heavily doped than the surface depletion region; and electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic

function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path, as can be seen at the right center of the figure.

Regarding claim 3, the circuitry comprises 2 inductors at the left center of the figure.

Regarding claim 8, the plate and body regions in figure 50C extend to a primary surface of the semiconductor body.

Regarding claims 11, 22, 31, 32, 33, 36, 37, and 42, Ikeda discloses in figure 46 electrode 26 and source 12 corresponding to the plate region are finger shaped.

Regarding claim 10, 34, the body region substantially laterally surrounds, and extends below substantially all of, the plate region.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4-6, 9, 12-19, 20, 21, 23-29, 30, 38, 39, 40, 41, and 43-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda as applied to claim 1 above, and further in view of Sedra and Smith, hereinafter Sedra (Microelectronic Circuits, page 382).

Regarding claim 4-7, 12-19, 23-28, and 43-46, Ikeda discloses the claimed invention except the plate to body bias voltage and the gate to body voltage is varied as a function of the plate to body voltage. Sedra discloses on page 382, figure 5.25, a FET transistor in which the drain plate and the gate are biased by a voltage VD, hence gate to body voltage is varied linearly, by a constant multiplier of 1, as a function of the plate to body voltage as the plate to body voltage is varied.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to connect the plate region in Ikeda's invention to the gate region, thus make a signal path, and further bias them together with a voltage, or separately bias the plate and the gate relative to the body in order to control the operation of the transistor.

Regarding claims 9, 20, 29, 38, 39, and 40, the plate region in figure 50C occupies a lateral plate area along the primary surface, and the capacitance dependency on the plate area, an inversion layer that meets the plate region occurs in the body region under control of the plate and gate electrodes, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area, all are inherent in the structure.

Regarding claims 21, 30, and 41, the body region substantially laterally surrounds, and extends below substantially all of, the plate region.

4. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda as applied to claim 32 above, and further in view of Imoto et al., hereinafter Imoto (U.S. 6,166,404).

Ikeda discloses the claimed invention except the insulating region extending into the semiconductor body. Imoto discloses insulation regions 81 of figure 1 in order to form electrically isolated areas in the substrate 51 (see column 4, lines 9-16). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include field insulating region into the semiconductor body in order to isolate the primary region.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on M-F 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703)306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Dana Farahani
March 7, 2002

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800